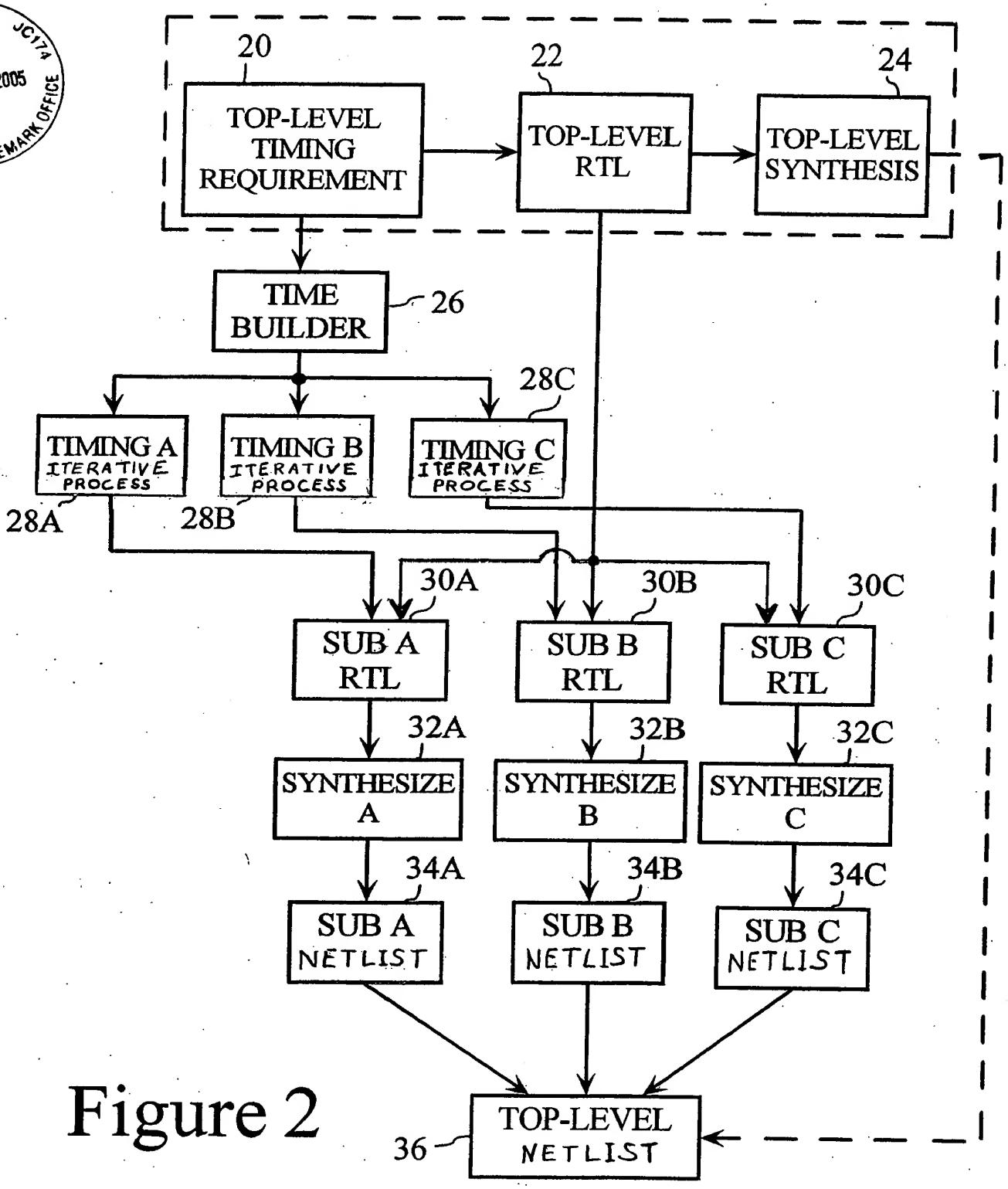

Figure 2

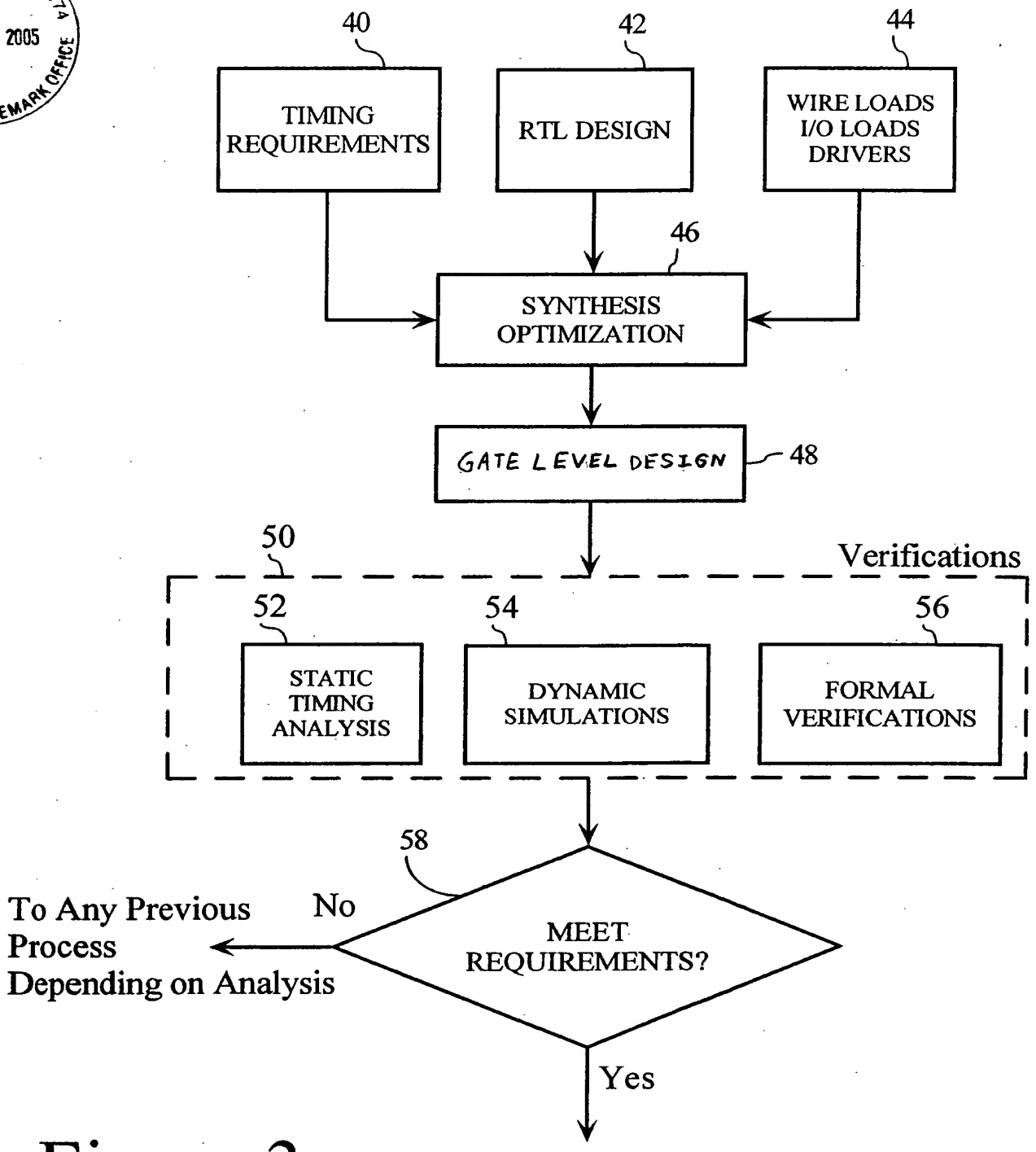

Figure 3 RTL Synthesis and Timing Optimization Complete

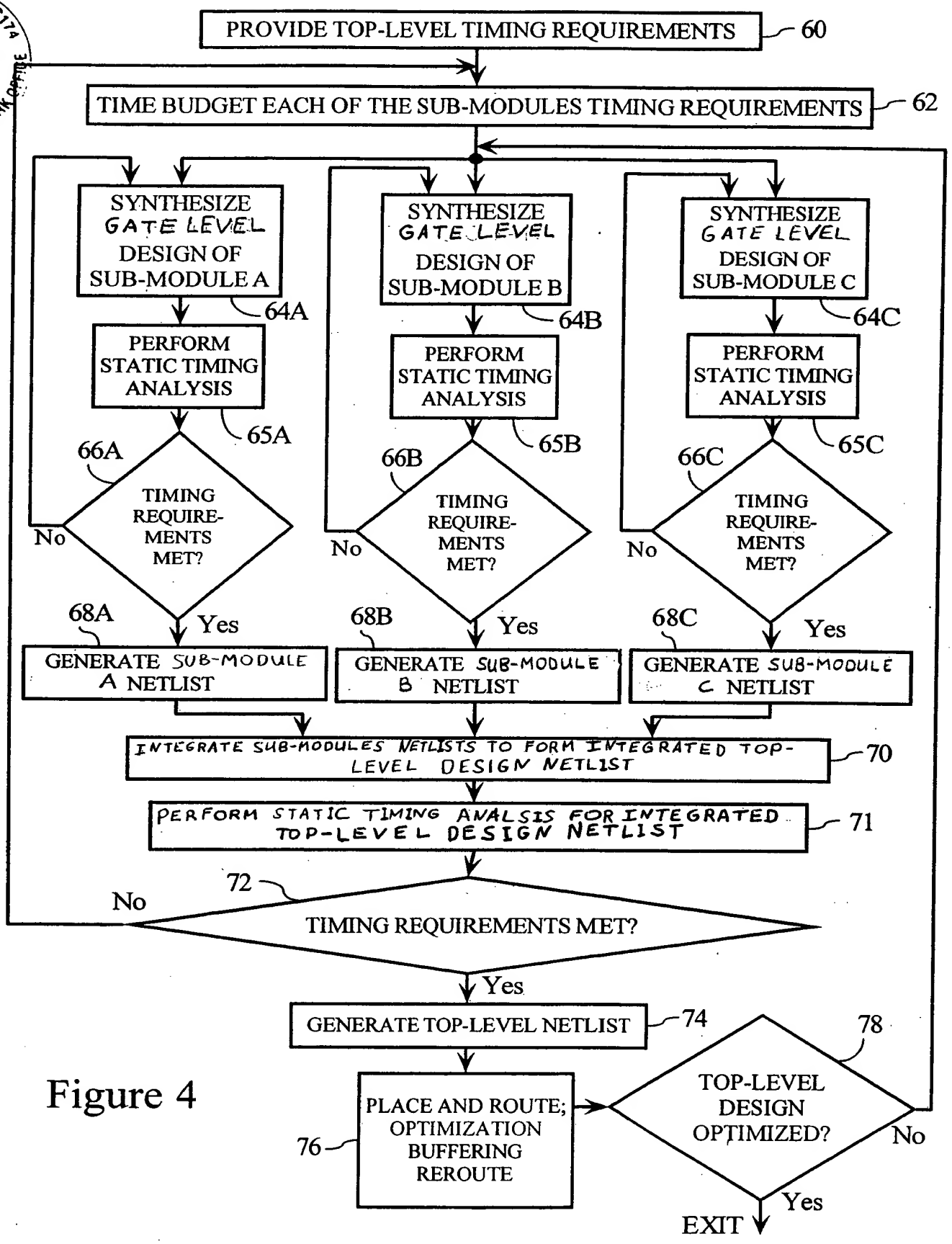

Figure 4